AF/2878 $

Practitioner's Docket No. ATM-181 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: R. Daniel McGrath et al.
Application No.: 09/872,209 Group No.: 2878
Filed: June 1, 2001 Examiner: S.K. Yam
For: DUAL-MODE CMOS INTEGRATED IMAGER HAVING USER INTERFACE (as amended)

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TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION—37 C.F.R. § 1.192)

NOTE: The phrase "the date on which" an "appeal was taken" in 35 U.S.C. 154(b)(1)(A)(ii) (which provides an adjustment of patent term if there is a delay on the part of the Office to respond within 4 months after an "appeal was taken") means the date on which an appeal brief under § 1.192 (and not a notice of appeal) was filed. Compliance with § 1.192 requires that: 1. the appeal brief fee (§ 1.17(c)) be paid (§ 1.192(a)); and 2.the appeal brief complies with § 1.192(c)(1) through (c)(9). See Notice of September 18, 2000, 65 Fed. Reg. 56366, 56385-56387 (Comment 38).

1. Transmitted herewith, in triplicate, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal filed on May 12, 2003.

NOTE: "Appellant must, within two months from the date of the notice of appeal under § 1.191 or within the time allowed for reply to the action from which the appeal was taken, if such time is later, file a brief in triplicate. . . " 37 C.F.R. § 1.192(a) (emphasis added).

CERTIFICATION UNDER 37 C.F.R. §§ 1.8(a) and 1.10*

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Date: October 10, 2003

Sally Azevedo
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** Only the date of filing (§ 1.6) will be the date used in a patent term adjustment calculation, although the date on any certificate of mailing or transmission under § 1.8 continues to be taken into account in determining timeliness. See § 1.703(f). Consider "Express Mail Post Office to Addressee" (§ 1.10) or facsimile transmission (§ 1.6(d)) for the reply to be accorded the earliest possible filing date for patent term adjustment calculations.*

10/17/2003 MAHMED1 00000033 09872209
02 FC:1253 950.00 OP

2. STATUS OF APPLICANT

This application is on behalf of

☒ other than a small entity.

☐ a small entity.

A statement:

☐ is attached.

☐ was already filed.

3. FEE FOR FILING APPEAL BRIEF

Pursuant to 37 C.F.R. § 1.17(c), the fee for filing the Appeal Brief is:

☐	small entity	$160.00
☒	other than a small entity	~~$320.00~~ 330.00

Appeal Brief fee due $ 330.00

4. EXTENSION OF TERM

NOTE: 37 C.F.R. § 1.704(b) ". . .an applicant shall be deemed to have failed to engage in reasonable efforts to conclude processing or examination of an application for the cumulative total of any periods of time in excess of three months that are taken to reply to any notice or action by the Office making any rejection, objection, argument, or other request, measuring such three-month period from the date the notice or action was mailed or given to the applicant, in which case the period of adjustment set forth in § 1.703 shall be reduced by the number of days, if any, beginning on the day after the date that is three months after the date of mailing or transmission of the Office communication notifying the applicant of the rejection, objection, argument, or other request and ending on the date the reply was filed. The period, or shortened statutory period, for reply that is set in the Office action or notice has no effect on the three-month period set forth in this paragraph."

NOTE: The time periods set forth in 37 C.F.R. § 1.192(a) are subject to the provision of § 1.136 for patent applications. 37 C.F.R. § 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

NOTE: As the two-month period set in § 1.192(a) for filing an appeal brief is not subject to the six-month maximum period specified in 35 U.S.C. § 133, the period for filing an appeal brief may be extended up to seven months. 62 Fed. Reg. 53,131, at 53,156; 1203 O.G. 63, at 84 (Oct. 10, 1997).

The proceedings herein are for a patent application and the provisions of 37 C.F.R. § 1.136 apply.

(complete (a) or (b), as applicable)

(a) ☒ Applicant petitions for an extension of time under 37 C.F.R. § 1.136 (fees: 37 C.F.R. § 1.17(a)(1)-(5)) for the total number of months checked below:

Extension (months)	Fee for other than small entity	Fee for small entity
☐ one month	$ 110.00	$ 55.00
☐ two months	$ 410.00	$ 205.00
☒ three months	$ ~~930.00~~ 950.00	$ 465.00
☐ four months	$ 1,450.00	$ 725.00
☐ five months	$ 1,970.00	$ 985.00

Fee: $ 950.00

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request $_____

or

(b) ☐ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal brief fee $ 330.00

Extension fee (if any) $ 950.00

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☐ Charge any additional fees required by this paper or credit any overpayment in the manner authorized above.

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NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to change the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, *1065 O.G. 31-33.*

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SIGNATURE OF PRACTITIONER

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(Text continued on page 9–55)

12/Appeal Brief 10-25-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant: R. Daniel McGrath et al.
Serial No.: 09/872,209 Group Art Unit: 2878
Filed: June 1, 2001 Examiner: S. K. Yam
For: DUAL-MODE CMOS INTEGRATED IMAGER HAVING USER INTERFACE (as amended)

Appeal Brief

Hon. Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

This brief is filed in support of Applicant's appeal of May 12, 2003. A petition for a 3-month extension of time together with payment of the fee therefor is submitted with this brief. Reversal of the Examiner's rejection of claims 1-9 is respectfully requested.

Table of Contents

1. Real Party in Interest

The applicants, R. Daniel McGrath, Bennett H. Rockney, Vincent S. Clark and Surinderjit S. Dhaliwal, who are the joint inventors of the claimed subject matter in this application, have assigned ownership of the subject invention and the application for patent to Atmel Corporation (reel 013680, frame 0492), by an instrument in writing recorded in the Patent and Trademark Office.

2. Related Appeals and Interferences

There are no known related appeal or interference cases.

3. Status of Claims

Claims 1-9 have been presented in this case.

Claims 1-9 are pending, have been rejected and are on appeal.

No claims have been allowed.

4. Status of Amendments

An amendment was filed after the Final Rejection of February 13, 2003 and it has been entered by the Examiner.

5. Summary of Invention

The claimed invention (see Fig. 1) is a CMOS integrated imager system (17) that allows a user to select one of two operating modes relating to timing control of an imager array (27). In a first operating mode (in which the imager system is capable of performing basic imaging functions in stand-alone operation), the system uses an internal timing element (31) to provide the timing signals for controlling the system's imaging operation. In a second operating mode (which provides the user with the option to take control of the timing, e.g. for more advanced imaging functions), the system bypasses (through bypass multiplexer 29) the internal timing element and timing signals are instead received (35) from an external timing generator (41). A mode signal (333, see Fig. 6) received from a user sets the operating mode of the system, for example by configuring a bypass multiplexer (29) to either interconnect or bypass the internal timing element's (31) connection to a control bus (35) that forms part of a user interface of the system. Thus, a user has complete control over the selection between internal and external timing modes of the system. The imager system may operate (claim 6) in the first operating mode as its default setting whenever its user interface is not connected to receive a mode signal.

The integrated imaging system has an imager array (27; see also Figs. 13 and 14) that is an array of pixel areas (900), which includes a plurality of light collecting elements. Each light collecting element (e.g., photodiode 907) receives light and stores electronic information in an amount indicative of an amount of light received during an integration period. The

timing signals, whether internal or external, determine, for example, scanning of the array and hence the integration period for each light collecting element. (cf., page 12, line 4 to page 13, line 10 of the specification)

The system also has at least one control area with a user interface. The control area might include such circuit elements as registers (21), analog-to-digital conversion (ADC) and correlated double sampling (CDS) blocks (23 and 25), a microcontroller (50, see Fig. 2), imager sensor logic (52), etc. But most important to the present invention is the aforementioned internal timing element (31), together with internal buses (35-37), especially the control bus 35 that carries timing signals, and the bypass multiplexer (29). (See claim 2.) The user interface (including ports 42-44) can receive a plurality of data, address and control signals and place them into the internal buses (35-57), which are electrically coupled to the interface. In particular, among the control signals that the user interface is configured to receive from a user is the aforementioned mode signal (333) and, when in the second operating mode, any timing signals from an external timing element (41). It is this mode signal that allows a user to select either an internal or an external timing source for the system.

The integrated imaging system may further include outboard logic (19), such as an FPGA (171; Fig. 5), that is electrically connected to the imager system (17; 117) for providing timing signals from an external timing element (41) when the system is operating in the second operating mode. This logic circuitry can include, for example, a memory and DMA

interface block (39) as well as an external timing generator and color recovery block (41). (cf., page 4, line 38 to page 5, line 11; page 7, line 29 to page 8, line 3). As noted above, the timing generator block (41) generates the external timing signals established by a user for customized imager operations, giving the user maximum flexibility and control. All timing is normally generated internally (from the internal timing element 31), but this outboard logic (19) makes the option available to take external control of every aspect of scan timing (such as by the external FPGA 171) when the user requires the modes of operation extended for advanced imaging beyond those basic imaging modes programmed into the imager (17).

6. Issues

(I) Whether claims 1-6 are unpatentable, under 35 U.S.C. 103(a), over Shinohara (European Patent Appln. No. EP 0942592) in view of Noble et al. (U.S. Patent No. 5,760,636).

(II) Whether claims 7-9 are unpatentable under 35 U.S.C. 103(a) in view of Shinohara.

7. Grouping of Claims

With respect to the first ground of rejection under 35 U.S.C. 103(a), claims 1-6 stand or fall together. With respect to the second ground of rejection under 35 U.S.C. 103(a), claims 7-9 stand or fall together.

8. Argument

A. Rejection of Claims 1-6 Under 35 U.S.C. 103(a)

The Shinohara patent teaches an image sensor chip 1 having an image pickup unit 30 containing plural photoelectric conversion elements and a reference clock generation circuit 7. With a externally connected microcomputer 2, the image sensor chip forms an image sensing unit that can reduce electrical power consumption by allowing the image sensor chip to perform some preliminary image capturing operation on its own. Once a necessary image is detected, the microcomputer is turned on to perform more sophisticated image processing tasks such as color processing or white balancing. (Column 4, lines 17-34). Since the microcomputer consumes much energy, reduction of its use save energy.

It is clear in the Shinohara patent that the microcomputer is an integral and indispensable part of the device - for every image, it completely takes over the image capturing process during a main operation once the preliminary operation has resulted in the detection of a necessary image. The internal clock on the image sensor chip 1 merely provides the drive pulses needed to perform the preliminary stage of image detection, then automatically transfers to the microprocessor clock for the main operation. The timing transfer is not a user selected mode. Every image capture operation requires the external microprocessor element, so that the image sensor chip 1 can not act as a stand-alone element. Shinohara's preliminary and main operations are not "user" established "modes", despite the

similar terminology, so much as successive stages in a single imaging operation.

This differs from the claimed invention in which the imager chip by itself has every element needed to provide high quality images using an easy interface and simple operation that allows the design and production of an image-capturing device with reduced time and cost. The present invention's claimed "user interface" also allows the user an option to connect an external FPGA to the image chip that can take control of every aspect of scan timing and thereby provide a more complex imaging device with extended capability. (Page 3, lines 11-24). However, the imager chip by itself, without an attached FPGA, is also sufficient with its claimed onboard "control area" and "internal timing element" to carry out complete imaging operations. The claimed "first mode" is not simply a preliminary operation in need of some subsequent mass operation performed by an essential microcomputer, as in Shinohara, but rather is a complete imaging operation. The outboard or external FPGA device that could be attached in the present invention for use in the claimed "second mode" is indeed optional. (Claims 7-9 recite the "outboard logic" as part of the system, whereas claims 1-6 recite only the imager having the "interface" that permits such as external element to be optionally connected.)

In essence, the claimed invention is an imaging chip with a built-in timing circuit that can be enabled or disabled at the option of a user by asserting a pin on the chip. This feature expands the versatility of the chip because it allows a product designer to use it as an all-in-one imaging chip that requires no additional processing circuitry to build a finished

product, or it can be used as a slave chip controlled by an advanced controller capable of issuing elaborate timing scheme for added functionality. For instance, a camera maker may simply connect the chip, with its internal timing enabled, to a memory module, a simple micro-controller and a shutter and then house it in a plastic enclosure with a lens system to build a simple and cost effective camera. Alternatively, the camera manufacturer may use the same chip, with its internal timing replaced by an FPGA, to build a sophisticated camera with advanced imaging features such as digital zooming and picture cropping. Moreover, as claimed, if a user desires to use one of the built-in functions ("first mode") of the imager chip the user can still select the first operation mode and ignore the timing from the FPGA.

With regards to this unique user interface, the Examiner concedes that "Shinohara does not teach the interface as a user interface configured to receive the mode signal from a user." (Office action, at 3).

The Examiner continues by stating that Noble et al. supplement the missing teaching of Shinohara. Specifically, with regard to Noble et al., the Examiner provides:

> Noble et al. teach [sic] (see Fig. 1) a microprocessor (10) with a user interface (12) wherein the clock frequency ("Clock Frequency") is adjusted based on a mode signal (SLOW#) received from a user (see Col. 3, lines 46-49 and Col. 6, lines 21-29) to provide user control of power consumption (See Col. 6, lines 24-29). It would have

> been obvious to one of ordinary skill in the art at the time the invention was made to use a user interface receiving a mode signal from a user as taught by Noble et al. in the system of Shinohara, to provide customized user control of power consumption to best suit a user's particular needs, as taught by Noble et al. (see Col. 6, lines 24-29). [quotes from Office action, at pages 3-4.]

Applicants respectfully disagree with the assertion that the missing teachings of Shinohara are supplemented by Noble et al. Noble et al. is concerned with a method for adjusting a clock frequency and voltage supplied to a processor via two signal lines which may be user supplied. In Noble (Fig. 1), a clock is coupled to and controls the frequency at which a processor operates. A voltage regulator is also coupled to the processor and determines the voltage at which the processor operates. Once the frequency of the clock is reduced, after receiving a SLOW_# signal which may be user sent, the frequency of the processor is reduced. The clock also communicates directly with the voltage regulator, telling the voltage regulator to lower the voltage supplied to the processor. The voltage operator complies, and the processor continues to operate in a low power mode. A POWER_READY signal received by the clock will raise the voltage. Therefore, in Noble et al., the user provides a signal that lowers the frequency of the clock. The user signal <u>does not bypass an internal timing element to externally control timing operation of the system</u>. The signal merely raises or lowers the frequency of the clock, thus the

frequency of the processor. This is not a user supplied mode signal of the type specified by the present claims. (Claim 1: "to receive from a user a mode signal for setting the system...")

If the Noble et al. teaching were to be combined with the Shinohara teaching, a user of Shinohara might, at best, be able to control the amount of voltage supplied to a processor via a timing element. But that is not the present claimed invention. Noble et al. fails to provide any teaching or suggestion that would direct one of skill in the art to provide a user signal that would cause the internal timing mode to be bypassed to control the timing operation of the system. Instead, Noble merely provides a teaching that would allow a user to decrease or increase the frequency of the clock, thus the voltage that would be supplied to a single processor. There is no teaching or suggestion in Noble to provide a user signal that would bypass the clock to control the timing operation of the system.

As it is clearly evidenced in the Shinohara disclosure, the goal of that patent document is to reduce power consumption. As for the Noble et al. patent, it teaches a method and apparatus for adjusting the clock frequency and voltage supplied to and integrated circuit in order to likewise reduce power consumption. As the goal of both prior art references is to conserve power, they could not have provided either suggestion or motivation to modify their teaching to arrive at the claimed invention. The object of the claimed invention which has to do with providing the functional flexibility to an imaging system, rather than power reduction, so as to be operable in either internal or external timing mode as controlled by a user.

In contrast, the present invention is drawn toward a user interface receiving a user mode signal for setting the system in one of a first operating mode using an internal timing element or of a second operating mode bypassing the internal timing element to control the timing operation of the system. Specifically, claim 1 recites, "a user interface for receiving a plurality of… signals, said interface configured to receive from a user a user mode signal for setting the system in one of a first operating mode or a second operating mode characterized in that the first operating mode uses the internal timing element to control timing operation of the system and the second operating mode bypasses the internal timing element to control timing operation of the system" (emphasis added).

As has been clearly shown, the Shinohara patent, taken as a whole, does not suggest the crucial elements of claimed subject matter in claim 1. The combination with Noble et al. patent does not advance the argument for rejection at all, as the Noble et al. patent does not teach the crucial missing element.

Therefore, Applicants respectfully submit that the rejection is in error and that it should be reversed. As claims 2-6 depend, either directly or indirectly upon claim 1, Applicants respectfully submit that the rejection to these claims should be reversed as well.

B. Rejection of Claims 7-9 Under 35 U.S.C. 103(a) as Being Obvious Over Shinohara

With regard to Shinohara, the examiner states, "Shinohara do [sic] not teach a user establishing timing signals

and a user interface allowing selection of the onboard timing means or outboard logic circuit." Office action, at 4. The Examiner continues, "[i]t would have been obvious for one of ordinary skill in the art at the time the invention was made to establish a user interface to allow selection of onboard timing means or outboard logic circuit and allow a user to establish timing signals in the timing selector of Shinohara, to allow user control of power consumption from the microprocessor and activation/deactivation of the image processing functions provided by the microprocessor to provide a more user-flexible system." Office action, at 5. Applicants respectfully disagree.

Shinohara is concerned with reducing power consumption in the solid state image pickup device by using a feedback mechanism wherein user control cannot be used. Shinohara provides a feedback mechanism whereby a switch is automatically shifted so that a signal from the microcomputer is supplied to the drive pulse generation circuit instead of a signal from the reference clock generation circuit. Specifically, Shinohara recites, "[t]he signals read from the sensor unit are entered into the image detection circuit, and, if the necessary image is detected, the output of the latch circuit is shifted to a high level state whereby the microcomputer is turned on. At the same time the switch 9 is shifted that the signal from the microcomputer is supplied to the drive pulse generation circuit." Shinohara, col. 4, lines 16-22. Additionally, Shinohara states:

> [I]n the preliminary operation, the preliminary operation mode generation circuit 8 generates a drive control signal of the

> preliminary operation mode based on the reference clock signal generated by the reference clock generation circuit 7 on the image sensor chip, and the drive pulse generation circuit 21 generates drive pulses based on the generated drive control signal to drive the peripheral scanning circuits. The image pickup unit sequentially reads out the image…. In the case that the image detection circuit 11 determines that the sensor receives the necessary image, the latch circuit 12 is latched. This determination may be attained by simple image detection, such as detection of an image signal component whose level is greater than a pre-determined level. In the preliminary operation, it is therefore possible in a scanning and read-out operation to reduce the number of horizontal and vertical scanning lines in image signal reading… or to perform the operation intermittently, since the sensor is operated as a monitor to merely determine whether or not the sensor receives the necessary image. The power consumption in this case can be significantly reduced not only in the microcomputer but also in the solid state image pickup device." Shinohara col. 4, line 46 to col. 5, lines 13 (emphasis added).

The Examiner states that it would have been obvious to establish a user interface to allow selection of onboard timing

means or outboard logic circuit in Shinohara. However, Applicants respectfully submit that an object of Shinohara is to reduce power consumption through use of the automated feedback mechanism of the sensor. Timing selection by the microcomputer is automatic at the appropriate time and is not a user selectable option. Therefore, if the feedback sensor of Shinohara were to be substituted with the "user interface allowing selection of the onboard timing means or outboard logic circuit," as recited in claim 7, Applicants submit that the principle of operation of Shinohara would be altered. This is not permissible when making an obviousness determination. The MPEP explicitly articulates this rule as follows:

> If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. M.P.E.P. § 2143.01, 2100-125 (August 2001) (citing *In re Ratti*, 123 U.S.P.Q. 349 (CCPA 1959)).

Therefore, Shinohara "neither teaches nor suggests" the claimed invention.

Further, Applicants respectfully submit that Shinohara fails to teach or suggest, as recited in Applicants' claim 7, "an outboard logic circuit electrically connected to the CMOS integrated imager generating signals established by a user for establishing user defined timing signals for customized imager operation…." There is no teaching or suggestion in Shinohara

that provides that the user customizes an imager operation by establishing signals. Applicants respectfully submit that "[m]odification unwarranted by the disclosure of a reference is improper." Carl Schenck, A.G. v. Nortron Corp., 218 U.S.P.Q. 698, 702 (Fed. Cir. 1983).

Therefore, Applicants respectfully submit that Shinohara fails to teach or suggest the teaching of claimed 7 and that the Examiner has erred in his rejection assertion for the reasons stated above. As claims 8-9 depend from claim 7, Applicants respectfully submit that the rejection to these claims should be reversed as well.

9. Conclusion and Relief Requested

The claims are nonobvious under U.S.C. 103(a) and are patentable over the prior art. Reversal of the Examiner's decision is earnestly requested.

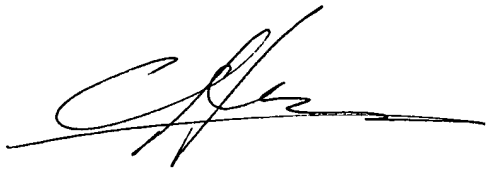
CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313

Signed: Sally Azevedo
Typed Name: Sally Azevedo

Date: October 10, 2003

Respectfully submitted,



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Appendix A - Claims on Appeal

1. An improved CMOS integrated imager system having an array of pixel areas with at least one control area, wherein said pixel areas include a plurality of light collecting elements which each receive light and store electronic information in an amount indicative of an amount of light received during an integration period, with the control area having an internal timing element, wherein the improvement comprises:

a user interface for receiving a plurality of data, address, and control signals, said interface configured to receive from a user a mode signal for setting the system in one of a first operating mode or a second operating mode characterized in that the first operating mode uses the internal timing element to control timing operation of the system and the second operating mode bypasses the internal timing element to control timing operation of the system.

2. The imager system of Claim 1, wherein the control area includes a data bus, an address bus and a control bus electrically coupled to the interface and further includes a bypass multiplexer connected to the control bus, said multiplexer operating to interconnect the internal timing element to the control bus upon receipt of a first mode signal and operating to bypass the internal control element upon receipt of a second mode signal.

3. The imager system of Claim 1, further including means for receiving timing signals from an external timing element when the system is operating in the second operating mode.

4. The imager system of Claim 3, wherein the external timing element includes an external timing generator and a color recovery block.

5. The imager system of Claim 3, wherein the external timing element includes a memory and a DMA interface block.

6. The imager system of Claim 1, wherein the imager operates in the first operating mode when the interface is not connected to receive the mode signal.

7. A timing selector for a CMOS integrated imager comprising:

an onboard timing means, associated with a CMOS integrated imager, for providing standard timing signals to operate a clock circuit aboard the integrated imager;

an outboard logic circuit electrically connected to the CMOS integrated imager generating signals established by a user for establishing user defined timing signals for customized imager operation, and

a user interface allowing selection of the onboard timing means or outboard logic circuit.

8. The apparatus of Claim 7, wherein the outboard logic circuit has means for generating clock signals bypassing the clock circuit.

9. The apparatus of Claim 7, wherein the outboard logic circuit has means for generating clock signals using the clock circuit.